



MAIN LOGIC BOARD SCHEMATIC

U.S. Patent #4,136,359
Other U.S. and Foreign patents pending.

NOTE:
1 PERIPHERAL CONNECTOR 0 DOES NOT GET I/O SELECT (PIN 1)
2 ON PERIPHERAL CONNECTOR 7 ONLY, PIN 19 IS CONNECTED TO SYNC (C13-B), AND PIN 35 IS CONNECTED TO COLOR REF (B13-2)

I/O SELECTS

4	E1	27	7	I/O 7 TO PIN 1, PERIPHERAL CONNECTOR 7	-	6
5	E2	26	9	I/O 6 TO PIN 1	-	5
6	E3	25	10	I/O 5 TO PIN 1	-	4
7	E4	24	11	I/O 4 TO PIN 1	-	3
8	E5	23	12	I/O 3 TO PIN 1	-	2
9	E6	22	13	I/O 2 TO PIN 1	-	1
10	E7	21	14	I/O 1 TO PIN 1	-	0
11	E8	20	15		-	

DEVICE SELECTS

4	E1	27	7	DEV 7 TO PIN 41 PERIPHERAL CONNECTOR 7	-	6
5	E2	26	9	DEV 6 TO PIN 41	-	5
6	E3	25	10	DEV 5 TO PIN 41	-	4
7	E4	24	11	DEV 4 TO PIN 41	-	3
8	E5	23	12	DEV 3 TO PIN 41	-	2
9	E6	22	13	DEV 2 TO PIN 41	-	1
10	E7	21	14	DEV 1 TO PIN 41	-	0
11	E8	20	15		-	

PERIPHERAL CONNECTOR (1 OF 8)

1	I/O SEL	+12V	50
2	D8	-49	51
3	A0	48	52
4	A2	47	53
5	A3	46	54
6	A4	45	55
7	A5	44	56
8	A6	43	57
9	A7	42	58
10	A8	41	59
11	A9	40	60
12	A10	39	61
13	A11	38	62
14	A12	37	63
15	A13	36	64
16	A14	35	65
17	A15	34	66
18	A16	33	67
19	R/W	32	68
20	INT IN	31	69
21	INT OUT	30	70
22	DMA OUT	29	71
23	DMA IN	28	72
24	+5V	27	73
25	GND	26	74

UNMARKED ON BOARD USER 1 JUMPER

1	RESET	13	14
2	INQ	12	13
3	FROM A7-3	11	12
4	RAB1	10	11
5	RESET	9	10
6	RESET	8	9
7	RESET	7	8
8	RESET	6	7
9	RESET	5	6
10	RESET	4	5
11	RESET	3	4
12	RESET	2	3
13	RESET	1	2